REMARKS

Claims 19-37 are pending.

Claims 19-37 stand rejected.

Claim 37 has been amended.

Claims 38-44 have been added.

No new matter has been added.

Claims 19-44 are hereby submitted for reconsideration.

In paragraphs 2 and 4 of the Office Action, the Examiner has rejected claim 37 under 35 U.S.C. §§ 112 and 132 for containing subject matter which was not disclosed in the original application as filed. Specifically, the Examiner states that the original specification does not disclose a cache memory being directly coupled to the first host processor. Applicants have amended claim 37 accordingly and respectfully request that this rejection be withdrawn.

In paragraph 6 of the Office Action, the Examiner has rejected claims 19-36 under 35 U.S.C. § 103 as being unpatentable over Reader et al. (U.S. Patent No. 6,192,073) in view of Kim (U.S. Patent No. 5926,187), further in view of Kusters (U.S. Patent No. 5,819,112). The Examiner contends that Reader teaches a first processor system, a second local processor, a cache subsystem, a data streamer, an interface unit, a plurality of external I/O devices and a data streamer receiving the output of VP, and the VP receiving the output of the data streamer, the scalar processor receiving the output of the data streamer, and the data streamer receiving the output of the scalar processor.

The Examiner further contends that Kim teaches a multimedia processor, the cache subsystem, control circuit, ROM cache, data caches and instruction caches as well as a data

transfer switch and a data streamer. It is contended that such a processors is similar to that of the Reader processor and that it would have been obvious to combine the inventions of Kim and Reader, with each reference claiming a different aspect of the same multimedia processor.

The Examiner continues by asserting that all of the elements of the present invention are taught by Kim and Reader except for a multiplexer, coupled to the interface, for providing access between a selected number of I/O device driver units to external I/O devices via output pins. However, the Examiner contends that Kusters teaches such an element and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multimedia processor of Reader with the multiplexer of Kusters to arrive at the present invention as claimed.

In paragraph 11 of the Office Action, the Examiner has alternatively rejected claims 19-36 under 35 U.S.C. § 103 as being unpatentable over Reader et al. (U.S. Patent No. 6,192,073) in view of Kim (U.S. Patent No. 5,926,187).

In paragraph 14 of the Office Action, the Examiner has provisionally rejected claims 19-36 under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-18 of co-pending U.S. Patent Application No. 09/172,286 now U.S. Patent No 6,347,344. Applicants hereby submit a terminal disclaimer, and respectfully request that this rejection be withdrawn.

Applicants respectfully disagree with the Examiner's contentions and submit the following remarks in response.

As discussed in the prior amendment, the present invention as claimed in claim 19, is directed to an integrated multimedia system having a multimedia processor disposed in an

integrated circuit, wherein the multimedia system comprises a first host processor system coupled to the multimedia processor. A second local processor is disposed within the multimedia processor for controlling the operation of the multimedia processor. A data transfer switch is disposed within the multimedia processor and coupled to the second processor for transferring data to various modules of the multimedia processor. A data streamer is coupled to the data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor, at least one of which is a cache memory, in accordance with corresponding channel allocations.

An interface unit is coupled to the data streamer having a plurality of input/output (I/O) device driver units. A multiplexer is coupled to the interface unit for providing access between a selected number of I/O device driver units to external I/O devices via output pins and a plurality of external I/O devices are coupled to the multimedia processor.

In this configuration, the present invention maintains a data streamer 122 which provides advantages over prior art systems in that it maintains the ability to schedule parallel (simultaneous) data transfers among a plurality of modules disposed within the multimedia processor by means of simultaneously establishing connections with a plurality of modules in accordance with the corresponding channel allocations. See pages 37-44 of description. To this end, the data streamer increases data transfer efficiency and further increases the processing efficiency of the processor.

The data streamer 122 is connected to the data transfer switch 112 and the interface unit 202. Thereby, the data transfer switch 122 can schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor as claimed in independent claims

19 and 28.

This configuration makes it possible for the data transfer switch of the present invention to perform simultaneous data transfers among all of the modules disposed within the multimedia processor. For example, a simultaneous data transfer can be performed between Interface 202, connected to an external I/O device, and memory controller 124, connected to external memory 128. At the same time, a data transfer between memory controller 124 and cache 108, connected to processor 102,104 can also be conducted, as claimed in new claims 39 and 40.

The cited prior art, namely Reader, teaches a method and apparatus for processing video data using three processors capable to operate concurrently, a scaler processor, a vector processor and a bit stream processor. Reader provides for vector coprocessor 220 that performs linear transformation and bitstream processor 245 that encodes/decodes input/output data to or from the vector processor 220 to perform distributed processing of multiple data streams.

In particular, as illustrated in Fig. 2 of Reader, bitstream processor 245 is coupled to IO BUS 240 and thus is connected to vector coprocessor 220 and scalar processor ARM7 RISC CPU 210.

As discussed in column 5, lines 4-36 of Reader, bitstream processor 245 receives data from vector compressor 220 via IO BUS 240 and cache subsystem 230, and transfers an operation result to scalar processor (CPU 210) via IO BUS 240 and cache subsystem 230. However, it is noted that bitstream processor is not coupled to FBUS 250 and thus is *not* connected to device interface 252, coupled with external devices, PCI bus interface 255 or memory controller 258 to schedule simultaneous transfers. Furthermore, vector coprocessor 220, not bitstream processor 245, if necessary, transfers data via FBUS 250 to external memory,

coupled with device interface 252 or memory controller 258. Accordingly, the bitstream processor 245 of Reader is a mere processor which encodes/decodes input/output data to or from vector coprocessor 220.

Contrary, to the Examiner's assertion, the data streamer 122 of the present inventions is not analogous to the bitstream processor 245 of the Reader reference. As discussed above, the data streamer of the present invention is capable of scheduling multiple simultaneous data transfers between all of the components of the multimedia processor, including the memory controller 124, and interface unit 202. On the contrary, the bitstream processor 245 of Reader is limited to processing functions with vector coprocessor 220 along the IO BUS 240.

As such, there is no teaching or suggestion in Reader that discloses the data streamer of the present invention. For example, there is no teaching or suggestion in Reader that discloses a data streamer coupled to the data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor, at least one of which is a cache memory, in accordance with corresponding channel allocations.

The cited Kim reference in Fig. 2 discloses a bitstream processor 246 similar to that disclosed in Reader, and is thus not analogous to the function of the data streamer 122 of the present invention for the same reasons stated above. The cited Kusters reference also does not teach a data streamer 122 within the meaning of the present invention.

Therefore, even if the three references were combined, the resulting structure would still not contain all of the elements claimed in the present invention. For example, there is no teaching or suggestion in any one of the cited references, either alone or in combination, that disclose a data streamer coupled to the data transfer switch, and configured to schedule

simultaneous data transfers among a plurality of modules disposed within the multimedia processor, at least one of which is a cache memory, in accordance with corresponding channel allocations.

As such, Applicants request that the rejection to the claims 19-37 be withdrawn and that new claims 38-44 not be subject to rejection and respectfully submit that the present invention as claimed is now in condition for allowance, the earliest possible notice of which is earnestly solicited. If the Examiner feels that a telephone interview would advance the prosecution of this application they are invited to contact the undersigned at the number listed below.

Respectfully submitted

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Dated: 6/20/03 By: _____

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